YHM2005/2006/2006A
Smart High Voltage Power Path with Special Features

Features

- Input work voltage range: 2.8V ~ 28V
- Input negative voltage Protection (down to -5.5V)
- Both VIN and VDD may supply the chip
- Ultra-low On-resistance: typical 20mΩ
- Power Path On/Off and discharge control
- Max 10V capability Gate to drive external NMOS
- Adjustable OVP (Over Voltage Protection)
  Default: 5.9V ± 200mV (YHM2006)
  No OVP (YHM2006A)
  11V ± 200mV (YHM2005)
- Optional active low (YHM2006 default on after POR) or high (YHM2005 default off after POR) enable pin for power switch
- Super-fast OVP response time: maximum 50ns
- 10-bits ADC for current sensing through power path，additional impedance & passive load short detection(through ENB) and VIN voltage
- Cable impedance and contact quality detection
- Active Short protection or high accuracy OCP
- Reverse current detection and protection
- Watch dog time-out to turn off power path and monitor MCU or AP as well
- UART communication between ENB and VIN or VOUT
- OTP (Over Temperature Protection with NTC)
- Robust ESD capability
- >2kV HBM & >1kV CDM
- 15kV air discharge & 8kV contact discharge under IEC 61000-4-2
- VIN tolerant to 35V clamping voltage during surge event.

Applications

- Mobile Phone, Tablet , Notebook, AR/VR Device，TWS, Wearable, Power Bank, Car Charger, Travel Adapter, Robot Cleaner and other power path, dual batteries and power monitor applications.

General Description

YHM2005/YHM2006 are Max 29V/4A smart power path products with ADC and I^2C support. The devices are super-fast response OVP with ultra-low resistance NMOS path.

YHM2006 active low default on to typically act as portable device input OVP function. YHM2005 active high default off to typically act as direct charge power path function.

YHM2005/YHM2006 support negative voltage input protection which can help to avoid damage while VBUS and GND exchange or other bad cases.

YHM2005/YHM2006 adopt special technology to measure the current through power path with high accuracy. It will help system to remove current detection resistance.

These chips integrate high side current source and low side current source which will do VIN pin impedance or moisture detection, VIN side discharge while power path off, cable impedance between power supply and portable device detection and VOUT side load resistance detection while power path off.

These chips also support watch dog function, once MCU or AP crash, the power path will be forced off, even may re-use GATE pin to reset MCU or AP as well.

One enhanced driver through GATE pin to control external NMOS by I^2C configuration.

Both of YHM2005 and YHM2006 come in a 3x4 array, 12-bump, 0.4mm pitch, 1.26mmx1.834mm wafer-level package (WLP).

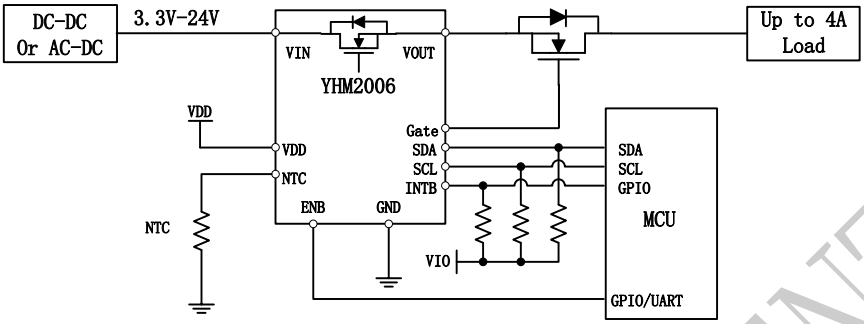


Fig 1. YHM2006 Typical Application_Smart Output with Reverse Blocking

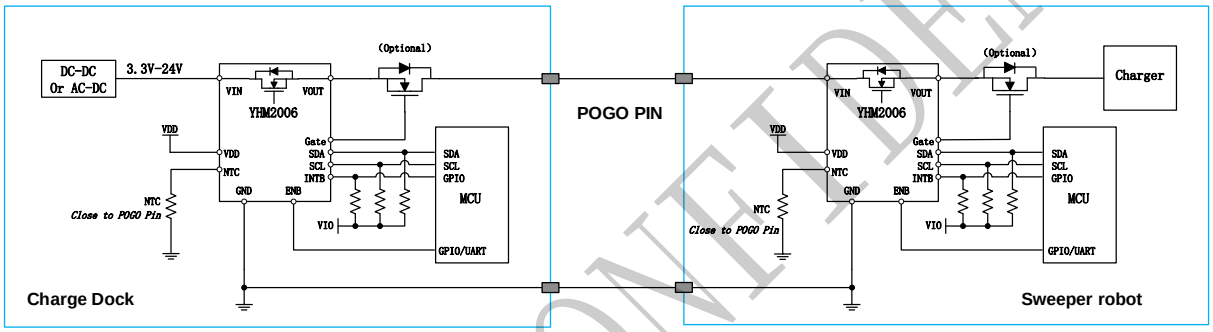


Fig 2. YHM2006 Typical Application_POGO Pin Smart Detection, Protection and Communication

YHM2005/YHM2006 Pin Configurations

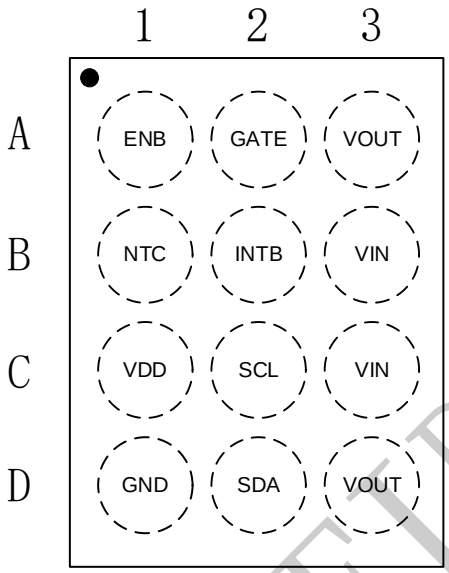


Fig 5. YHM2005/6WBT Pin Assignment (Top Through View)

YHM2005/YHM2006 WLP Pin Descriptions

WLP	Name	Description
A1	ENB	**Enable Input/Detection/UART**: Enable Active LOW/High by part number or optional Impedance Detection. Note: Enable Active Low: YHM2006, High: YHM2005. This pin can be configured for UART communication between VIN or VOUT.
B1	NTC	**NTC:** Connect NTC for over temperature protection.
C1	VDD	Chip Supply while VIN less than VDD.
D1	GND	**Ground**
A2	GATE	**Gate driver:** Charge-pump to drive external NMOS FET's Gate Independently or **Watch dog out to reset controller**
B2	INTB	**Current's Voltage/NTC Comp/Interruption output**: Current to voltage with amplifying analog output, or may set as NTC pin's comparator's output. Or Interruption viz Open-drain output Pull down to ground when any FLAG register alarms.
C2	SCL	**Serial Clock Input:** Be used to synchronize data movement on the I^2C serial interface, Tied GND for external OVP threshold set-up by SDA pin.
D2	SDA	**Serial Data Input/Output:** Input / Output pin for the 2-wire serial interface. Open-drain output and requires an external pull-up resistor. Adjustable OVP setting while SCL tied GND.
A3, D3	VOUT	**Power Output**: Power Path Output to Load.
B3, C3	VIN	**Power Input**: Power Path Input and Chip Supply.

1 Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameters		Min.	Max.	Unit
V_{IN}	VIN to GND		-5.5	29	V
V_{OUT}	VOUT to GND		-0.3	V_{IN} + 0.3	V
V_{GATE}	GATE to GND		-5.5	29	V
V_{VDD}	VDD to GND		-0.3	6.0	V
V_{IO}	Maximum DC Voltage Allowed on ENB, NTC, SCL, SDA and INTB		-0.3	6.0	V
I_{IN}	Switch I/O Current (Continuous)			11	A
t_{PD}	Total Power Dissipation at T_A=25°C			TBD	W
T_{STG}	Storage Junction Temperature		-65	+150	°C
T_J	Operating Junction Temperature			+125	°C
T_L	Lead Temperature (Soldering, 10 Seconds)			+260	°C
θ_{JA}	Thermal Resistance, Junction-to-Ambient (645mm^2 pad of 1oz. copper)				°C/W
ESD	Electrostatic Discharge Capability	Human Body Model, EIA/JESD22-A114	2		kV
		Charged Device Model, JESD22-C101	1		
	IEC61000-4-2 System Level	Air Discharge	15		
		Contact Discharge	8		

Note 1. Measured using 2S2P JEDEC std. PCB

2 Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance.

Parameters	Min.	Max.	Unit
Supply Voltage: V_{IN}	2.8	28	V
Supply Voltage: V_{DD}	3.0	5.5	V
GATE as NMOS Driver	-5.5	28	V
I^2C: SD and SCL	1.5	5.5	V
I/O pins: ENB, NTC, SCL, SDA, INTB and GATE as WD OUTPUT	0	5.5	V
Ambient Operating Temperature, T_A	-40	85	°C
VIN Capacitor	0.1		μF
VOUT Load Capacitor	0.1	1000	μF

3 Detailed Electrical Characteristics

Unless otherwise noted, V_{IN} =2.5 to 28V, T_A= -40 to 85°C; Typical values are at V_{IN} = 5.0 V, I_{IN} ≤ 3 A, C_{IN} = 0.1μF and T_A = 25ºC.

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Unit
Basic Operation (Refer to active low version YHM2006)						
I_Q	Input Quiescent Current on VIN	V_{IN} = 5V, ENB = 0V, 0x01 = 8'h00		150		μA
		V_{IN} = 20V, ENB = 0V, 0x01 = 8'h00		250		
	Input Quiescent Current on VDD	V_{DD} = 3.3V, ENB = 0V, 0x0E=8'h62 (INTB is interrupt)		10		
		V_{DD} = 3.3V, ENB = 0V, VIN = 0V (Default INTB is ISNS output)		30		
I_{IN_Q}	OVLO Supply Current	V_{IN} = 20V, V_{OUT} = 0V 06h[1:0]=2'b00		150		μA
I_{ADC}	VDD Current consumption of ADC	V_{DD} = 3.3V, ENB = 0V, 0x01 = 8'hC0, 0x07 = 8'h00, 0x08 = 8'hF0			1	mA
I_{SHDN}	Device shutdown current	V_{IN} = 5V, ENB = 3.3V, V_{OUT} = 0V		5	10	μA
I_{LEAK}	VIN Leakage current during detection (2)	V_{IN} = 2.1V, V_{OUT} = 0V, T_A = 65°C, DET_EN = 1, I_{SRC} = 0A;		30	100	nA
$V_{IN\_UV\_R}$	Under-Voltage Rising Trip Level	V_{IN} rising, T_A = -40 to 85°C	2.5	2.6	2.8	V
$V_{IN\_UV\_F}$	Under-Voltage Falling Trip Level			2.5		V
$V_{VDD\_UV\_F}$	Internal Under-Voltage Falling Trip Level for VDD	V_{DD} falling, T_A = -40 to 85°C	2.6	2.8	3.0	V
V_{HYS_VDD}	UVLO Hysteresis for VDD			100		mV
V_{IN_OVLO}	Internal Over-Voltage Trip Level (YHM2006 default), refer to register table for other value set by I²C	V_{IN} Rising, T_A= -40 to 85°C	5.7	5.9	6.1	V
V_{IN_OVLO}	Internal Over-Voltage Trip Level (YHM2005 default), refer to register table for other value set by I²C	V_{IN} Rising, T_A= -40 to 85°C	10.8	11	11.2	V
V_{OVLO_TH}	OVLO set threshold		1.18	1.204	1.22	V
V_{HYS_OVLO}	OVLO Hysteresis			2		%
V_{OV_RNG}	Adjustable OVLO	the voltage of SDA to trigger OVLO under VSCL <0.325V and V_{SDA} >0.25V	4		23	V
R_{ON}	Resistance from V_{IN} to	V_{IN} = 5V, I_{OUT} = 500mA, T_A = 25°C		20		mΩ

	V_{OUT}					
I_{OCP}	Default Over Current Protection threshold (2)	V_{IN} = 5V, T_A= 0 to 65°C		4		A
T_{SD}	Thermal Shutdown (2)			150		°C
T_{SH}	Thermal Shutdown Hysteresis (2)			20		°C
R_{PD}	Pull-down resistor on ENB			2		MΩ
I/O and Interface						
V_{OL_INTB}	INTB Output Low Voltage	I_{INTB} = 1mA, Interrupt Asserted			0.4	V
V_{IH_ENB}	ENB HIGH Voltage	V_{IN} = 2.8V to V_{IN_OVLO}	1.2			V
V_{IL_ENB}	ENB LOW Voltage	V_{IN} = 2.8V to V_{IN_OVLO}			0.5	V
I_{OUT_LEAK}	Leakage Current of INTB	V_{INTB} = 3V, Interrupt De-asserted			0.5	µA
I²C Interface						
V_{IH_I2C}	HIGH voltage of I²C input		1.2			V
V_{IL_I2C}	LOW voltage of I²C input				0.4	V
V_{OL_SDA}	LOW voltage of SDA				0.4	V
f_{SCL}	SCL clock frequency	Fast Mode		400		kHz
t_{BUF}	Bus Free Time Between STOP and START conditions (2)	Fast Mode		1.3		µs
$t_{HD;STA}$	START or Repeated START Hold Time (2)	Fast Mode		600		ns
t_{LOW}	LOW Period of SCL Clock (2)	Fast Mode		1.3		µs
t_{HIGH}	HIGH Period of SCL Clock (2)	Fast Mode		600		ns
$t_{SU;STA}$	Repeated START Setup Time (2)	Fast Mode		600		ns
$t_{SU;DAT}$	Data Setup Time (2)	Fast Mode		100		ns
$t_{HD;DAT}$	Data Hold Time (2)	Fast Mode	0		900	ns
t_{RSCL}	SCL Rising Time (2)	Fast Mode	20+0.1 Cb		300	ns
t_{RSDA}	SDA Rising Time (2)	Fast Mode	20+0.1 Cb		300	ns
t_{FSDA}	SDA Falling Time (2)	Fast Mode	20+0.1 Cb		300	ns
$t_{SU;STO}$	Stop Condition Setup Time (2)	Fast Mode		600		ns

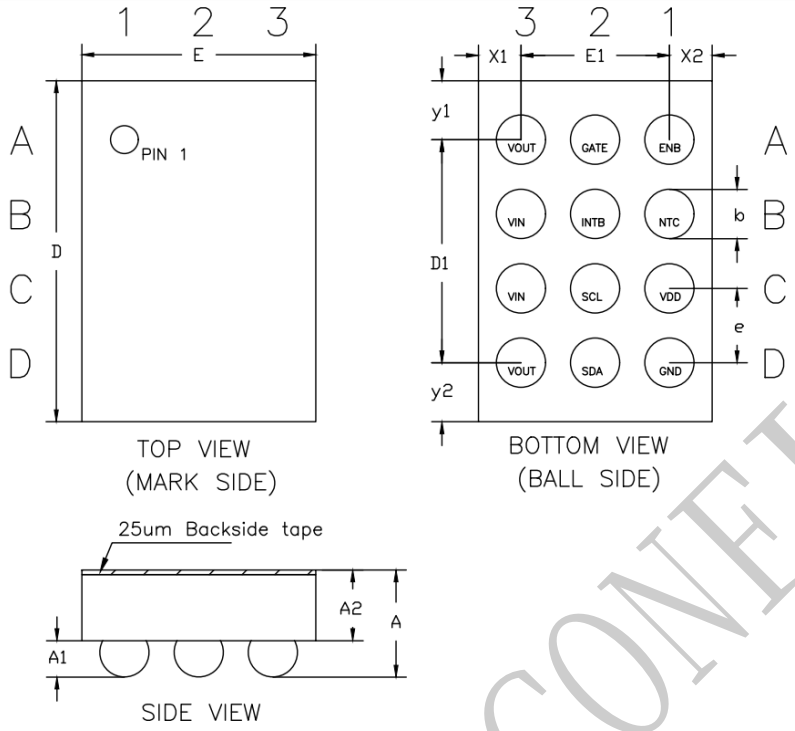
Cb	Capacitive Load for SDA and SCL				400	pF
t_{SP}	Pulse width of spikes which must be suppressed by input filter (2)		0		50	ns
Moisture Detection						
I_{SRC}	Current source applied on VIN for moisture detection	Set by register: 07h	0.001		11	mA
V_{DET_VIN}	VIN side detection voltage range		0.6		1.8	V
V_{DET_ENB}	ENB side detection voltage range		0.1		1.8	V
V_{SRC}	Clamping voltage on VIN in detection mode. Note:Scan VIN, test sink current from VIN, once the current from 10mA step by step drop to 5mA,at the time VIN voltage as V_{SRC}	VDD = 3.3V	1.8		2.2	V
I_{OD}	Current needed to over-drive VIN	VDD = 3.3V, ENB = 0V, 0x01 = 8'hC0, 0x07 = 8'h00, 0x08 = 8'h00, apply current on VIN to VOUT rises			40	mA
t_{SET}	Settle time for I_{SRC} and ADC (2)			40	60	µs
Timing Characteristics						
t_{OCP_QUAL}	OCP qualification time	From $I_{SW} > I_{OCP}$ to turning off action		50		µs
t_{OCP_RST}	OCP switch auto-restart time	Time from power switch turned off (OCP) to being turned on		100		ms
t_{INTB}	Interrupt maximum duration			1000		ms
t_{SW_DEB}	De-bounce Time of Power Switch turned on	Time from $2.5V < V_{IN} < V_{IN\_OVLO}$ to $V_{OUT} = 0.1 \times V_{IN}$		10		ms
t_{TAG_DEB}	De-bounce Time of register TAG_STS	Time from $VIN > V_{TH\_VIN}$ to $V_{INTB} = 0.1V$		250		µs
t_{UV_DEB}	De-bounce Time of Under Voltage Release (2)	VDD = 3.3V, ENB = 0V, 0x01 = 8'hC0		9		µs
t_{SS}	Soft-Start Time (2)(3)	Time from de-bounce time finished to Power Switch fully turn on		10		ms
t_R	Switch Turn-On rising Time	$V_{IN} = 5V$, $R_L = 100\Omega$, $C_L = 22\mu F$, V_{OUT} from $0.1 \times V_{IN}$ to $0.9 \times V_{IN}$,		2		ms
t_{OFF}	Switch Turn-Off Time (2)	Internal OVP configuration		50		ns

	R_L = 10Ω, C_L = 0μF, time from V_{IN} > V_{OVLO} to V_{OUT} = 0.1 × V_{IN}	External OVP configuration		100		

Note 2. This parameter is guaranteed by design and characterization; not production tested.
Note 3. Over Current Protection will be screened during this period.

Package Dimensions

WLCSP-12 1.260x1.834x0.574



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.529	0.574	0.619
A1	0.176	0.196	0.216
A2	0.353	0.378	0.403
D	1.814	1.834	1.854
D1		1.200BSC	
E	1.240	1.260	1.280
E1		0.800BSC	
b	0.245	0.265	0.285
e		0.400BSC	
x1		0.230 REF	
x2		0.230 REF	
y1		0.317 REF	
y2		0.317 REF	

Ordering Information

Part Number	Temp Range	Pin Package	Top Mark	MOQ
YHM2005WBT	-40°C to 85°C	12 WLCSP	YHM2005 YYWW LOTID	3000
YHM2006WBT	-40°C to 85°C	12 WLCSP	YHM2006 YYWW LOTID	3000
YHM2006AWBT	-40°C to 85°C	12 WLCSP	YHM2006 YYWW LOTID	3000

T = Tape and reel.
YYWW: Date Code. YY = year, WW = week.
LOTID: The last five number of LOTID.